

# JEEHO RYOO

Assistant Professor

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## RESEARCH INTERESTS

- Computer architecture, memory systems, and operating systems
- Performance, energy efficiency, and hardware/software co-design
- Emerging workload and system characterization

## EDUCATION

The University of Texas at Austin, College of Engineering, Austin, TX May 2017  
Doctor of Philosophy in Electrical and Computer Engineering  
Advisor: Lizy K. John

The University of Texas at Austin, College of Engineering, Austin, TX May 2014  
Master of Science in Electrical and Computer Engineering  
Advisors: Lizy K. John

Cornell University, College of Engineering, Ithaca, NY May 2011  
Bachelor of Science in Electrical and Computer Engineering  
Advisors: David H. Albonese and Christopher Batten

## ACADEMIC EXPERIENCES

Assistant Professor May 2024 – Present  
Gildart Haase School of Computer Sciences and Engineering, Fairleigh Dickinson University, Vancouver, BC

Adjunct Professor July 2023 – April 2024  
Gildart Haase School of Computer Sciences and Engineering, Fairleigh Dickinson University, Vancouver, BC

Research Associate March 2023 – April 2024  
Laboratory for Computer Architecture, The University of Texas at Austin, Austin, TX

Faculty August 2021 – April 2024  
British Columbia Institute of Technology, Vancouver, BC, Canada

## PROFESSIONAL EXPERIENCES

Senior Performance Engineer February 2018 – March 2019  
ARM Inc., San Jose, CA

- Implemented DRAM cache simulation infrastructure modeling future ARM server systems
- Developed caching and prediction schemes tailored for emerging memory technology

Senior Software Engineer July 2017 – February 2018  
Oracle Corporation, Santa Clara, CA

- Identified bottleneck in Transparent Huge Pages (THP) when running enterprise applications
- Analyzed cloud application performance across various hardware platforms

Research Engineering Intern May 2016 – December 2016  
Advanced Micro Devices, Austin, TX

- Proposed granularity aware migration schemes in heterogeneous memory systems
- Implemented dynamic granularity migration schemes on Linux kernel running on real x86-64 systems

Research Engineering Intern September 2015 – December 2015  
Advanced Micro Devices, Austin, TX

- Proposed bandwidth efficient and high capacity utilization die-stacked DRAM management policy
- Developed heterogeneous memory simulation platform incorporating emerging memory technologies

Software Engineering Intern May 2013 – August 2013  
Oracle Corporation, Santa Clara, CA

- Proposed hardware-assisted, software-managed die-stacked DRAM management policy
- Evaluated the proposed scheme with commercial benchmarks such as SPECjbb, SPECjEnterprise, TPC-C

Performance Architecture Intern May 2012 – August 2012  
 Samsung Austin R&D Center, Austin, TX

- Developed the Simpoint tool for ARM ISA to analyze various Android benchmarks
- Evaluated various power-efficient floating point schedulers using the Gem5 simulator

Graduate Research Assistant August 2011 – May 2017  
 Laboratory for Computer Architecture, The University of Texas at Austin, Austin, TX

- Proposed management policies for high bandwidth, low latency die-stacked DRAM technology
- Developed other uses of die-stacked DRAM such as a large TLB in virtual platforms

Undergraduate Research Assistant June 2010 – May 2011  
 Computer Systems Laboratory, Cornell University, Ithaca, NY

- Developed a digital ASIC tool-flow chain to synthesize the Verilog MIPS R10K microprocessor model
- Incorporated clock gating techniques at the functional block level (e.g. ALU, ROB) for power efficiency

Project Team Co-Director – Big Red Chip September 2010 – May 2011  
 Computer Systems Laboratory, Cornell University, Ithaca, NY

- Designed a superscalar OOO processor and on-board I/O interfaces on Xilinx Virtex-6 FPGA
- Provided project design guidelines for 5 sub-design teams and managed the project deadline

## TEACHING EXPERIENCES

Assistant Professor in the School of Computer Sciences and Engineering  
 Fairleigh Dickinson University, Vancouver, BC

- CSCI 6806 – Computer Science Graduate Capstone Project (Summer 2024)
- CSCI 5565 – Assembly Programming (Summer 2024)

Adjunct Professor in the School of Computer Sciences and Engineering  
 Fairleigh Dickinson University, Vancouver, BC

- CSCI 5565 – Assembly Programming (Spring 2024)
- CSCI 5565 – Assembly Programming (Spring 2024)
- CSCI 5565 – Assembly Programming (Summer 2023, Fall 2023, Spring 2024)

Faculty in the School of Computing and Academic Studies  
 British Columbia Institute of Technology, Vancouver, BC

- COMP 2510 – Procedural Programming in C (Winter 2022, Fall 2022, Winter 2023, Fall 2023)
- COMP 3522 – Object Oriented Programming 2 (Fall 2021, Winter 2022)
- COMP 4736 – Introduction to Operating Systems (Winter 2023)
- COMP 4800 – Projects Practicum 2 (Spring 2023)
- COMP 7035 – Operating Systems (Fall 2023)

Teaching Assistant

Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX

- EE306 (Instructor: Yale Patt) – Introduction to Computing (Fall 2011)
- EE382N (Instructor: Lizy John) – Performance Evaluation and Benchmarking (Fall 2014)
- EE460N (Instructor: Mattan Erez) – Computer Architecture (Spring 2012)

Teaching Assistant

Electrical and Computer Engineering, Cornell University, Ithaca, NY

- ENGRD2300 (Instructors: David H. Albonese, Adam W. Bojanczyk, José F. Martinez, and Edward G. Suh) – Introduction to Digital Logic Design (Spring 2010, Fall 2010, Spring 2011)

## PUBLICATIONS

Kumar, Shvetha S., Reshma R. Nayak, Jismi S. Kannampuzha, Sahil Rai, **Jeoho Ryoo**, and Lizy K. John. "Evaluation of Pruning Techniques." In 2023 IEEE International Performance, Computing, and Communications Conference (IPCCC), November, 2023.

Jensen, Steffen, Jaekyu Lee, Dam Sunwoo, Matt Horsnell, Matthew Sigs, **Jeoho Ryoo**, and Lizy John. "Do Video Encoding Workloads Stress the Microarchitecture?." In 2023 IEEE International Symposium on Workload Characterization (IISWC), October, 2023.

**Je Ho Ryoo**, Shuang Song and Lizy K. John, "Puzzle Memory: A Multifractional Partitioned Heterogeneous Memory Scheme." *In the Proceedings of 2018 International Conference on Computer Design (ICCD)*, October, 2018.

**Jee Ho Ryoo**, Lizy K. John, and Arkaprava Basu, “A Case for Granularity Aware Page Migration.” *In the Proceedings of 2018 International Conference on Supercomputing (ICS)*, June, 2018.

Yashwant, Marathe, Nagendra Gulur, **Jee Ho Ryoo**, Shuang Song and Lizy K. John, “CSALT: Context Switch Aware Large TLB.” *In the Proceedings of 2017 International Symposium on Microarchitecture (MICRO)*, October, 2017.

**Jee Ho Ryoo**, Nagendra Gulur, Shuang Song and Lizy K. John, “Rethinking TLB Designs in Virtualized Environments: A Very Large Part-of-Memory TLB.” *In the Proceedings of 2017 International Symposium on Computer Architecture (ISCA)*, June, 2017.

**Jee Ho Ryoo**, Mitesh R. Meswani, and Lizy K. John, “SILC-FM: Subblocked InterLeaved Cache-Like Flat Memory Organization.” *In the Proceedings of 2017 International Conference on High Performance Computer Architecture (HPCA)*, February, 2017.

Mohammad Faisal Iqbal, Jim Holt, **Jee Ho Ryoo**, Gustavo de Veciana and Lizy K. John, "Dynamic Core Allocation and Packet Scheduling in Multicore Network Processors." *In IEEE Transactions on Computers*, vol. 65, no. 12, December, 2016.

**Jee Ho Ryoo**, Mitesh R. Meswani, Reena Panda, and Lizy K. John, “SILC-FM: Subblocked InterLeaved Cache-Like Flat Memory Organization.” *In the Proceedings of 2016 International Conference on Parallel Architecture and Compilation Techniques (PACT)*, September, 2016. (Poster)

Shuang Song, Meng Li, Xinnian Zheng, **Jee Ho Ryoo**, Reena Panda, Michael LeBeane, Andreas Gerstlauer, and Lizy K. John, “Proxy-Guided Load Balancing of Graph Processing Workloads on Heterogeneous Clusters.” *In the Proceedings of 2016 International Conference on Parallel Processing (ICPP)*, August, 2016.

Reena Panda, Xinnian Zheng, **Jee Ho Ryoo**, Michael LeBeane, Shuang Song, Andreas Gerstlauer, and Lizy K. John, “Genesys: Automatically Generating Representative Training-sets.” *In the Proceedings of 2016 International Conference on Embedded Computer Systems: Architecture, Modeling, and Simulation (SAMOS)*, July, 2016.

Michael LeBeane, Shuang Song, Reena Panda, **Jee Ho Ryoo** and Lizy K. John, “Data Partitioning Strategies for Graph Workloads in Heterogeneous Clusters.” *In the Proceedings of 2015 International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, November, 2015.

**Jee Ho Ryoo**, Karthik Ganesan, Yao-Min Chen and Lizy K. John, “i-MIRROR: A Software Managed Die-Stacked DRAM-Based Memory Subsystem.” *In the Proceedings of 2015 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, October, 2015.

Michael LeBeane, **Jee Ho Ryoo**, Reena Panda and Lizy K. John, “WattWatcher: Fine-Grained Power Estimation For Emerging Workloads.” *In the Proceedings of 2015 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, October, 2015.

Reena Panda, Christopher Erb, Michael LeBeane, **Jee Ho Ryoo** and Lizy K. John, “Performance Characterization of Modern Databases on Out-of-order CPUs.” *In the Proceedings of 2015 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, October, 2015.

**Jee Ho Ryoo**, Saddam Quirem, Michael LeBeane, Reena Panda, Shuang Song and Lizy K. John, “GPGPU Benchmark Suites: How Well Do They Sample the Performance Spectrum.” *In the Proceedings of 2015 International Symposium on Parallel Processing (ICPP)*, September, 2015. **(Best Paper Runner-Up)**

Wooseok Lee, Youngchun Kim, **Jee Ho Ryoo**, Dam Sunwoo, Andreas Gerstlauer and Lizy K. John, “PowerTrain: A Learning-based Calibration of McPAT Power Models.” *In the Proceedings of 2015 International Symposium on Low Power Electronics and Design (ISLPED)*, July, 2015.

**Jee Ho Ryoo**, Michael LeBeane, Mohammad Faisal Iqbal and Lizy K. John, “Control Flow Behavior of Cloud Workloads.” *In the Proceedings of 2014 International Conference on Workload Characterization (IISWC)*, October, 2014. (Poster)

Mohammad Faisal Iqbal, Jim Holt, **Jee Ho Ryoo**, Gustavo De Veciane and Lizy K. John, “Flow Migration on Multicore Network Processors: Load Balancing While Minimizing Packet Reordering.” *In the Proceedings of 42nd International Conference on Parallel Processing (ICPP)*, October, 2013.

Jinsuk Chung, Ikhwan Lee, Michael Sullivan, **Jee Ho Ryoo**, Don Wan Kim, Doe Hyun Yoon, Larry Karplan and Mattan Erez, “Containment Domains: A Scalable, Efficient, and Flexible Resilience Scheme for Exascale Systems.” *In the Journal of Scientific Programming*, vol. 21, no. 3-4, 2013.

Jinsuk Chung, Ikhwan Lee, Michael Sullivan, **Jee Ho Ryoo**, Don Wan Kim, Doe Hyun Yoon, Larry Karplan and Mattan Erez, “Containment Domains: A Scalable, Efficient, and Flexible Resilience Scheme for Exascale Systems.” *In the Proceedings of 2012 International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, November, 2012.

## INVITED TALKS

“Future of Computing and AI Impact,” Vancouver Korean IT Conference, Vancouver, BC, July 15, 2023

## SERVICES

#### Technical Program Committee

- IEEE International Conference on Performance, Computing and Communications (IPCCC): 2024

#### Reviewer

- ACM Computing Surveys: 2024
- IEEE Transactions on Computers (TC): 2015
- Simulation Modelling Practice and Theory (SIMPAT): 2016

#### Student Volunteer

- IEEE International Symposium on Workload Characterization (IISWC): 2011
- ACM/SPEC International Conference on Performance Engineering (ICPE): 2015

### **PATENTS**

Intelligently Partitioning Data Cache to Allocate Space for Translation Entries, Lizy K. John, **Jee Ho Ryoo**, Yashwant Marathe, Nagendra Gulur.

US Patent 10261915B2

Methodology to Utilize Heterogeneous Memories with Variable Properties, Lizy K. John, **Jee Ho Ryoo**, Hung-Ming Hsu, Karthik, Ganesan.

US Patent 20180260323A1

Page-Migration with Varying Granularity. Arkaprava Basu, and **Jee Ho Ryoo**.

US Patent 10503658B2

Processor Using a Level 3 Translation Lookaside Buffer Implemented in Off-Chip or Die-Stacked Dynamic Random-Access Memory. Lizy K. John, Nagendra Gulur, and **Jee Ho Ryoo**.

US Patent 10296465B2

Data Block Sizing for Channels in a Multi-Channel High-Bandwidth Memory. **Jee Ho Ryoo**, and Mitesh R. Meswani.

US Patent 10503655B2

Low Latency, High Bandwidth Memory Subsystem Incorporating Die-Stacked DRAM. **Jee Ho Ryoo**, Karthik Ganesan, and Yao-Min Chen.

US Patent 9406361B2

### **AWARDS**

Samsung Award of Excellence (2012) – Intern award recipient for excellent work performance

Engineering Learning Initiatives (2010) – Motorola research funding recipient for two semesters

Roger Berman '70 Memorial Prize (2010) – Top presentation student in engineering communications program